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REMARKS

Claims 1, 2, 7-10, 15-18, 23-26, 31-34, 39 and 40 have been amended. Claims 1-40 remain pending in the application. No new matter has been added. Applicants respectfully request reconsideration in view of the forgoing amendments and these remarks.

I. Interview

Applicants wish to thank the Examiner for an in person interview that was conducted with Applicant's representative and the Examiner on July 11, 2006. During the interview the Itoh and Caspar references were discussed with reference to claim 1. No agreement was reached.

II. Allowable claims

Applicants wish to thank the Examiner for indicating that claims 2-5, 7, 8, 10-13, 15, 16, 18-21, 23, 24, 26-29, 31, 32, 34-37, 39 and 40 were merely objected to as being dependent upon a rejected base claim, but would otherwise be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicants have amended these claims to include the underlying limitations and believe that these claims as such are in condition for allowance.

III. Claim Objection

Claim 18 has been objected to because of an informality. Applicants have amended claim 18 to correct the noted informality.

IV. 35 USC 103 Rejection

Claims 1, 6, 9, 14, 17, 22, 25, 30, 33 and 38 stand rejected under 35 USC 103(a) as being unpatentable over Itoh (United States Patent Number 4, 667, 166, hereinafter referred to as "Itoh") in view of Casper (United States Patent number 6, 420, 932 hereinafter referred to as "Casper"). Applicants respectfully traverse the rejection.

a. Claim 1 and its dependent claims

Claim 1 is directed to an amplifier that is operable to receive an input signal and a feedback signal and produce an intermediate signal. The amplifier includes a variable-offset circuit that is operable to receive the intermediate signal and produce an output signal and the

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feedback signal. The output signal has a DC offset that varies corresponding to a varying parameter of the variable-offset circuit. Further, the amplifier is operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifier.

The Examiner has suggested that Itoh teaches all of the limitations set forth in claim 1 with the exception of a variable offset circuit, which the Examiner suggests is taught by Casper. Applicant respectfully disagrees. Applicants respectfully submit that neither Itoh nor Casper teaches or suggests Applicants' claimed 1) amplifier that is operable to reduce variation of the DC offset of an output signal by a factor that corresponds to a gain of the amplifier or 2) variable offset circuit.

Itoh shows an amplifier circuit in Fig. 3. The amplifier circuit 66 is connected to a transistor 16 and provides a feedback loop from the emitter of transistor 16 to an input of the amplifier 66 (Itoh shows a similar configuration for a second input of the differential circuit and includes amplifier 68 and transistor 18). As discussed in Itoh, the amplifier 66,68 ensures that the emitter voltage at the output of transistor 16,18 is identical to the input signal received (see Itoh, Col 5, line 32-38). By doing such, Itoh is able to maintain collector currents associated with the output of the circuit to be free of drift and distortion (See Itoh, Col. 5, line, 45-49). Itoh does not define or describe the gain of the amplifier 66,68 or any relationship of the gain to a property or effect in the circuit proposed. Applicants respectfully assert that Itoh fails to teach or suggest Applicants' claimed amplifier configuration that is operable to reduce a variation of a DC offset of an output signal by a factor that corresponds to a gain of the amplifier. As discussed above, Itoh makes no mention of gain, DC offset or reduction of the DC offset by either a fixed or variable amount. Further, Applicants respectfully assert that the reduction of DC offset is not inherent in the structure shown in Itoh. As set forth in Applicant's claimed structure, Applicants' amplifier is configured such that it is operable to reduce the variation of the DC offset of the output signal by a factor that corresponds to its gain. Itoh does not teach or suggest any such configuration. Further, as admitted by the Examiner, Itoh fails to teach or suggest Applicants' claimed variable offset circuit.

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Casper fails to cure the defects of Itoh. The Examiner has suggested that Casper is Applicants' claimed variable offset circuit. Applicants respectfully disagree for at least the following reasons: 1) There is no motivation to combine Casper and Itoh in the manner proposed by the Examiner, and therefore the combination is improper, 2) even if combined, the combination of Itoh and Casper fails to teach or suggest a variable offset circuit that produces an output signal having a DC offset that varies corresponding to a varying parameter of the variable offset circuit.

Applicants respectfully assert that there is no motivation or reason to combine the teachings of Itoh and Casper. As an initial matter, Applicants are unclear with respect to how the Examiner proposes to combine the teachings of Casper with Itoh. The Examiner has suggested that Casper includes Applicants' claimed variable offset circuit (indicating that elements 114 and 116 of Casper Fig. 1 are Applicants' claimed variable offset circuit). Applicants respectfully assert that elements 114 and 116 are merely variable current sources. Accordingly, Applicants are unclear where or how the Examiner proposes to include the variable current sources in Itoh, or why such inclusion would be necessary. Applicants respectfully assert that Itoh is completely functional as presented and would not need nor require such a substitution or addition. Itoh makes no mention of a need for variability in its design, and accordingly Applicants can find no motivation for the same. Applicants respectfully assert that such a combination is improper.

Further, even if motivation were found and a combination proposed (which Applicants respectfully assert that the Examiner has failed to do), Applicants respectfully assert that Casper's variable current sources 114, 116 fail to teach or suggest Applicants' claimed variable offset circuit that is configured to produce an output signal having a DC offset that varies in accordance with a varying property of the variable offset circuit. Casper's variable current sources 114, 116 source or sink current and provide no DC offset adjustment (notably, as current is adjusted in the variable current source 114, 116, Applicant can find no indication or teaching of any DC offset adjustment that is provided). Accordingly, Applicants respectfully assert that the combination of Itoh and Casper fails to teach or suggest Applicants' claimed variable offset

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circuit that that is configured to produce an output signal having a DC offset that varies in accordance with a varying property of the variable offset circuit.

Claim 6 depends from claim 1 and is allowable for at least the same reasons set forth above with respect to claim 1.

b. Claim 9 and its dependent claims

Claim 9 is directed to a circuit that includes an amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal and a processing means for receiving the intermediate signal and producing an output signal and the feedback signal. The output signal has a DC offset that varies corresponding to a varying parameter of the processing means. The amplifying means is operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifying means.

Claim 9 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 14 depends from claim 9 and is allowable for at least the same reasons set forth above with respect to claim 9.

c. Claim 17 and its dependent claims

Claim 17 is directed to a wireless transceiver and includes a receiver operable to receive a modulated carrier signal. The receiver includes an amplifier operable to receive an input signal and a feedback signal and produce an intermediate signal and a variable-offset circuit operable to receive the intermediate signal and produce an output signal and the feedback signal. The output signal has a DC offset that varies corresponding to a varying parameter of the variable-offset circuit. The amplifier is operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifier.

Claim 17 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 22 depends from claim 17 and is allowable for at least the same reasons set forth above with respect to claim 17.

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d. Claim 25 and its dependent claims

Claim 25 is directed to a wireless transceiver that includes a receiver means for receiving a modulated carrier signal. The receiver means includes amplifying means for receiving an input signal and a feedback signal and producing an intermediate signal and processing means for receiving the intermediate signal and producing an output signal and the feedback signal. The output signal has a DC offset that varies corresponding to a varying parameter of the processing means. The amplifying means is operable to reduce variation of the DC offset of the output signal by a factor that corresponds to a gain of the amplifying means.

Claim 25 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 30 depends from claim 25 and is allowable for at least the same reasons set forth above with respect to claim 25.

e. Claim 33 and its dependent claims

Claim 33 is directed to a method for reducing variation of a DC offset that includes amplifying an input signal to produce an intermediate signal, processing the intermediate signal to produce a feedback signal and an output signal, the output signal having a DC offset that varies corresponding to a varying parameter of circuitry used to process the intermediate signal and reducing variation of the DC offset of the output signal using the feedback signal by a factor that corresponds to a gain of the amplification.

Claim 33 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 38 depends from claim 33 and is allowable for at least the same reasons set forth above with respect to claim 33.

V. 35 USC 103 Rejection

Claims 17 and 25 stand rejected under 35 USC 103(a) as being unpatentable over Kasperkovitz (PCT Publication WO 02/071604), (hereinafter referred to as "Kasperkovitz") in view of Itoh and further in view of Casper. Applicants respectfully traverse the rejection.

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a. Claim 17

Kasperkovitz does not cure the deficiencies of Itoh and Casper. Kasperkovitz provides no details of its amplifier structure. For at least the reasons set forth above with regard to claims 1 and 17, Applicants respectfully assert that claim 17 is allowable.

b. Claim 25


Kasperkovitz does not cure the deficiencies of Itoh and Casper. Kasperkovitz provides no details of its amplifier structure. For at least the reasons set forth above with regard to claims 1 and 25, Applicants respectfully assert that claim 25 is allowable.

Applicants respectfully request a three-month extension of time up to and including September 13, 2006.

Enclosed is a credit card authorization for excess claim fees and for the Petition for Extension of Time fee for responding to the outstanding action up and until September 13, 2006.

Respectfully submitted,

Date: 9-12-2006


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